CLAIMS

I claim:

1. In a dynamic random access memory device, having a complementary-logic bitline pair having true and inverted bitlines:

equilibrating means, connected to the bitline pair; and

biasing means, connected to only one of the bitlines;

wherein when said equilibrating and biasing means are activated together, the bitline pair is thus equilibrated and biased.

2. The device of claim 1, wherein:

said equilibrating means comprises a first transistor, connected to the bitline pair, such that when activated, the bitlines are shorted together;

said biasing means comprises a second transistor, connected to only one of the bitlines and connected to a biasing node, such that when activated, the one of said bitlines is shorted to said biasing node;

such that when said first and second transistors are activated together, said bitline pair is equilibrated and biased.

3. The device of claim 2, wherein said biasing node is located next to said second transistor.

4. The device of claim 2, wherein said biasing node is connected to a current-limiting device, and wherein an n-channel substrate contact can be located next to said current-limiting device without widening circuit area.

5. The device of claim 2, wherein an n-channel contact can be located next to said biasing node, without widening circuit area.

6. In a dynamic random access memory device, having a biasing node, and first and second complementary-logic bitline pairs each having a true and an inverted bitline:

first equilibrating means, able to short the bitlines of the first bitline pair together;

second equilibrating means, able to short the bitlines of the second bitline pair together;

first biasing means, able to short only one of the bitlines of the first bitline pair to the biasing node;

second biasing means, able to short only one of the bitlines of the second bitline pair to the biasing node;

wherein the biasing node is interstitially located between said first and second biasing means.

7. The device of claim 6, wherein:

said first equilibrating means comprises a first transistor, connected to the first bitline pair, such that when said first transistor is activated, the first bitline pair is shorted together;

said second equilibrating means comprises a second transistor, connected to the second bitline pair, such that when said second transistor is activated, the second bitline pair is shorted together;

said first biasing means comprises a third transistor, connected to only one of the bitlines in the first bitline pair and connected to a biasing node, such that when said third transistor is activated, the one of said bitlines of the first bitline pair is shorted to said biasing node;

said second biasing means comprises a fourth transistor, connected to only one of the bitlines in the second bitline pair and connected to said biasing node, such that when said fourth transistor is activated, the one of said bitlines of the second bitline pair is shorted to said biasing node;

wherein said first, second, third, and fourth transistors are activated together, thus equilibrating and biasing the bitline pair.

8. The device of claim 7, wherein said biasing node is connected to a current-limiting device, and wherein an n-channel substrate contact can be located next to said current-limiting device without widening circuit area.

9. The device of claim 7, wherein an n-channel contact can be located next to said biasing node, without widening circuit area.

10. In a dynamic random access memory device, having:

an equilibrate node;

a biasing node;

a complementary-logic bitline pair having true and inverted bitlines;

a first transistor, connected to said bitline pair and gated by said equilibrate node such that when said equilibrate node is activated, said bitline pair is shorted together and thus equilibrated;

a second transistor, connected to said true bitline and to said biasing node, and gated by said equilibrate node, such that when said equilibrate node is activated, said true bitline is shorted to said biasing node, thus biasing said true bitline;

a third transistor, connected to said inverted bitline and to said biasing node, and gated by said equilibrate node, such that when said equilibrate node is activated, said inverted bitline is shorted to said biasing node, thus biasing said inverted bitline;

the improvement comprising:

conversion of one of said second and third transistors from a three-terminal device to a two-terminal device, allowing said biasing node to be located next to

remaining unconverted of said second and third transistors, without widening circuit area.

11. The device of claim 10, wherein said biasing node is connected to a current-limiting device, and wherein an n-channel substrate contact can be located next to said current-limiting device without widening circuit area.

12. The device of claim 10, wherein an n-channel contact can be located next to said biasing node, without widening circuit area.

13. In a dynamic random access memory device, having:

an equilibrate node;

a biasing node;

a complementary-logic bitline pair having true and inverted bitlines;

a first transistor, connected to said bitline pair and gated by said equilibrate node such that when said equilibrate node is activated, said bitline pair is shorted together and thus equilibrated;

a second transistor, connected to said true bitline and to said biasing node, and gated by said equilibrate node, such that when said equilibrate node is activated, said true bitline is shorted to said biasing node, thus biasing said true bitline;

a third transistor, connected to said inverted bitline and to said biasing node, and gated by said equilibrate node, such that when said equilibrate node is activated, said inverted bitline is shorted to said biasing node, thus biasing said inverted bitline;

the improvement comprising:

elimination of one of said second and third transistors, allowing said biasing node to be located next to remaining of said second and third transistors, without widening circuit area.

14. The device of claim 13, wherein said biasing node is connected to a current-limiting device, and wherein an n-channel substrate contact can be located next to said current-limiting device without widening circuit area.

15. The device of claim 13, wherein an n-channel contact can be located next to said biasing node, without widening circuit area.